10/629221

C of C

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent No.: 6,885,227 B2

Issued: April 26, 2005

First Named Inventor: Om P. Agrawal

Title: CLOCK GENERATOR WITH SKEW CONTROL

Certificate
JUL 28 2005
of Correction

REQUEST FOR EXPEDITED ISSUANCE OF CERTIFICATE OF CORRECTION PURSUANT TO 37 CFR 1.322

Certificate of Corrections Branch
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Review of the above-identified patent has revealed errors in the claims attributable solely to the Patent and Trademark Office. Applicant therefore requests that a Certificate Of Correction be issued to correct these errors.

The location of the errors in the patent and the corresponding correct language in the application file are set forth below:

Error in Patent	Correct Language in Application File
Col. 11, lines 37 (claim 11)	Amendment filed 10/08/04, claim 11, line 2

Documentation supporting this request and a form PTO/SB/44 showing the corrections are enclosed.

Although no fees are believed due, the Commissioner is hereby authorized to charge any fees associated with this communication to Deposit Account No. 501958.

Respectfully submitted,

Date: 7/21/05

By: _____

Mark L Becker
Associate General Counsel, IP
Reg. No. 31,325
Customer No. 29416

Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, OR 97124
Phone: 503-268-8629
Fax: 503-268-8077

PTO/SB/44 (04-04)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,885,227 B2

DATED : April 26, 2005

INVENTOR(S) : Agrawal et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 11, line 37: "the, output" should read -- the output--.

MAILING ADDRESS OF SENDER:
Lattice Semiconductor Corporation
5555 NE Moore Court
Hillsboro, OR 97124

PATENT NO. 6,885,227 B2

No. of additional copies

JUL 29 2005

an output circuit adapted to select from the plurality of second signals and provide at least one output signal; and

a skew control circuit adapted to selectively apply skew to the output signal by a third programmable amount, wherein the first, second, and third programmable amounts and the programmable frequencies are determined by data selected from electrically erasable memory.

2. The clock generator of claim 1, wherein the feedback signal is selected from an internal feedback signal and an external feedback signal, the skew control circuit further adapted to selectively apply skew to the internal feedback signal by a fourth programmable amount.

3. The clock generator of claim 1, wherein the skew control circuit may be selectively bypassed.

4. The clock generator of claim 1, wherein the skew comprises coarse adjustments or fine adjustments.

5. The clock generator of claim 1, wherein the output signal comprises two, single-ended signals or a differential signal, and the skew applied to each of the single-ended signals by the skew control circuit may differ.

6. The clock generator of claim 1, wherein a control signal determines the data selected from the electrically erasable memory.

7. The clock generator of claim 1, further comprising input/output boundary scan circuits adapted to provide JTAG test support for the clock generator.

8. The clock generator of claim 7, wherein the JTAG test support provides IEEE 1149.1 compliance.

9. The clock generator of claim 1, wherein the clock generator is in-system programmable.

10. The clock generator of claim 9, wherein the clock generator is in-system programmable by supporting IEEE 1532 standards.

11. The clock generator of claim 1, wherein the output circuit is further adapted to provide the, output signal over a range of selectable voltage levels, signal types, and output impedances, and the input circuit is further adapted to receive the input signal having a possible range of voltage levels and signal types.

12. An integrated circuit comprising:

means for selecting from a plurality of input signals and generating a first input signal having a configurable frequency;

means for selecting from a plurality of feedback signals and generating a second input signal having a configurable frequency;

a phase-locked loop core adapted to receive the first input signal and the second input signal and generate a first signal;

means for receiving the first signal and generating a plurality of second signals having configurable frequencies;

means for selecting from the second signals and providing a plurality of output signals; and

means for selectively skewing each of the output signals and at least one of the feedback signals.

13. The integrated circuit of claim 12, wherein the skewing comprises coarse adjustments or fine adjustments.

14. The integrated circuit of claim 12, further comprising means for providing configurability and in-system programmability.

15. The integrated circuit of claim 12, further comprising means for testing the integrated circuit to provide IEEE 1149.1 compliance.

16. The integrated circuit of claim 12, further comprising means for selecting the configurable frequency for the first input signal and the second input signal and the configurable frequencies for the second signals.

17. The integrated circuit of claim 12, wherein the input signals have a possible range of voltage levels and signal types, and the output signals each have a programmable voltage level and signal type.

18. The integrated circuit of claim 17, wherein the signal type comprises single-ended signals and differential signals.

19. A method of generating clock signals, the method comprising:

receiving an input signal, wherein the input signal may be a single-ended signal type or a differential signal type;

modifying a frequency of the input signal by an amount determined from a first set of data selected from memory to provide a first input signal;

receiving a feedback signal;

modifying a frequency of the feedback signal by an amount determined from a second set of data selected from the memory to provide a second input signal;

aligning a frequency and/or a phase of the first input signal and the second input signal to provide a first signal;

modifying a frequency of the first signal to generate a plurality of second signals having frequencies determined from a third set of data selected from the memory;

selecting from the second signals a plurality of output signals, which have programmable voltage levels and signal types; and

applying skew to the output signals by an amount determined from a fourth set of data selected from memory.

20. The method of claim 19, wherein the amount of the skew is based on coarse steps or fine steps.

21. The method of claim 19, further comprising providing in-system programmability to modify the first, second, third, and fourth set of data stored in the memory.

22. The method of claim 19, wherein a control signal selects the first, second, third, and fourth set of data stored in the memory.

23. The method of Claim 19, further comprising providing JTAG compliant functional testing.

24. A clock generator comprising:

an input circuit adapted to receive an input signal and provide the input signal to a phase-locked loop;

a phase-locked loop (PLL) adapted to receive the input signal from the input circuit and to generate in response an output signal;

an output circuit adapted to receive the output signal from the PLL and provide the output signal as a clock signal;

a first skew control circuit coupled to the PLL and adapted to generate a set of coarse skew adjustments and a set of fine skew adjustments; and

a second skew control circuit programmable to select and apply one of the skew adjustments to the output signal.

25. The clock generator of claim 24, wherein the second skew control circuit includes:

a plurality of registers programmable to store different skew selection signals;

a first multiplexer coupled to the registers and adapted to select one of the stored skew selection signals; and

a second multiplexer coupled to the first skew control circuit and to the first multiplexer and adapted to select a skew adjustment based on the skew selection signal selected by the first multiplexer.

9. (Original) The clock generator of Claim 1, wherein the clock generator is in-system programmable.

10. (Original) The clock generator of Claim 9, wherein the clock generator is in-system programmable by supporting IEEE 1532 standards.

11. (Original) The clock generator of Claim 1, wherein the output circuit is further adapted to provide the output signal over a range of selectable voltage levels, signal types, and output impedances, and the input circuit is further adapted to receive the input signal having a possible range of voltage levels and signal types.

12. (Original) An integrated circuit comprising:

means for selecting from a plurality of input signals and generating a first input signal having a configurable frequency;

means for selecting from a plurality of feedback signals and generating a second input signal having a configurable frequency;

a phase-locked loop core adapted to receive the first input signal and the second input signal and generate a first signal;

means for receiving the first signal and generating a plurality of second signals having configurable frequencies;

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049